

Attorney Docket No. 10004440-1

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (currently amended) ~~A computer-readable storage medium having~~
2 ~~computer-executable instruction set for initiating a~~ A computer-implemented
3 method of driving the simulation testing of a design of an integrated circuit (IC)
4 which is to be incorporated into an intended system comprising the steps of:
5 providing an asynchronous sequence of states configured for
6 simulating operating conditions relevant to driving sequencing of signal-
7 exchange events with said IC;
8 identifying first upper and first lower parameters of timing
9 constraints imposed by said intended system with respect to enabling
10 individual said events;
11 forming a first synchronous sequence of states in which said
12 states are synchronized on a basis of remaining within said first upper and
13 first lower parameters of timing constraints;
14 identifying second upper and second lower parameters of timing
15 constraints imposed by said IC with respect to enabling individual said events;
16 forming a second synchronous sequence of states in which said
17 states are synchronized on a basis of remaining within said second upper and
18 said second lower parameters of timing constraints; and
19 using said second synchronous sequence as a basis for said
20 simulation testing of said design.
- 1 2. (currently amended) ~~A computer-readable storage medium having~~
2 ~~computer-executable program code configured to implement a~~
3 A computer-implemented method of generating a synchronous sequence of
4 test vectors from information originating within an asynchronous environment
5 comprising:
6 providing a simulation synchronous sequence of states,
7 wherein each of said states is referenced to a clock period, said simulation
8 synchronous sequence being partially based on event timing parameters of
9 a particular system of interest;

10 introducing short timing delays to said states within specific said
11 clock periods of said simulation synchronous sequence to generate an
12 asynchronous short-delay sequence of states, durations of specific said short
13 timing delays being responsive to event timing parameters of a particular
14 Integrated circuit (IC) design;
15 comparing said states of said asynchronous short-delay
16 sequence, including correlating a plurality of said clock periods having said
17 states of said asynchronous short-delay sequence to identify a first over-
18 lapping time interval, said first overlapping time interval being consistent with
19 a time coincidence among said states of said asynchronous short-delay
20 sequence;
21 generating a synchronous short-delay sequence by successively
22 repeating a first delay-adjusted clock period having a state which is delayed
23 by said first overlapping time interval;
24 introducing long timing delays to said states within specific
25 said clock periods of said simulation synchronous sequence to generate
26 an asynchronous long-delay sequence of states, durations of specific said
27 long timing delays being responsive to event timing parameters of said
28 particular IC design;
29 comparing said states of said asynchronous long-delay
30 sequence, including correlating a plurality of said clock periods having said
31 states of said asynchronous long-delay sequence to identify a second
32 overlapping time interval, said second overlapping time interval being
33 consistent with a time coincidence among said states of said asynchronous
34 long-delay sequence;
35 generating a synchronous long-delay sequence by successively
36 repeating a second delay-adjusted clock period having a state which is
37 delayed by said second overlapping time interval; and
38 comparing said synchronous short-delay sequence with timing
39 of said states of said synchronous long-delay sequence to generate said
40 synchronous sequence of test vectors, including time aligning said
41 synchronous short-delay and long-delay sequences to detect a plurality of
42 overlapping sampling time intervals for locating said synchronous sequence of
43 test vectors.

1 3. (currently amended) ~~The storage medium~~ The computer-implemented
2 method of claim 2 wherein said step of introducing said short timing delays
3 includes adding best case tester-load timing delays to said clock periods of
4 said simulation synchronous sequence, said best case tester-load timing
5 delays being indicative timing constraints of an IC tester.

1 4. (currently amended) ~~The storage medium~~ The computer-implemented
2 method of claim 2 wherein said step of introducing said short timing delays
3 includes adding best case chip-load timing delays Indicative of timing
4 constraints of said IC design.

1 5. (currently amended) ~~The storage medium~~ The computer-implemented
2 method of claim 3 wherein said step of introducing said long timing delays
3 includes adding worst case tester-load timing delays that are Indicative of said
4 timing constraints of said IC tester.

1 6. (currently amended) ~~The storage medium~~ The computer-implemented
2 method of claim 4 wherein said step of introducing said long timing delays
3 includes adding worst case chip-load timing delays indicative of said timing
4 constraints of said IC design.

1 7. (currently amended) ~~The storage medium~~ The computer-implemented
2 method of claim 2 wherein said step of providing said simulation synchronous
3 sequence includes:

4 providing a simulated asynchronous sequence of states;
5 extracting a state of said asynchronous sequence at each said
6 clock period to generate a simulated synchronous sequence of states;
7 introducing an abbreviated timing delay to each said clock
8 period of said simulated synchronous sequence to generate a simulated
9 synchronous abbreviated-delay sequence and introducing an extended timing
10 delay to each said clock period of said simulated synchronous sequence to
11 generate a simulated synchronous extended-delay sequence; and
12 comparing said simulated synchronous abbreviated-delay
13 sequence to said simulated synchronous extended-delay sequence, including
14 time aligning said simulated synchronous abbreviated-delay and extended-
15 delay sequences to detect a plurality of overlapping second time intervals
16 for defining positions of states in said clock periods of said simulation
17 synchronous sequence.

1 8. (currently amended) ~~The storage medium~~ The computer-implemented
2 method of claim 7 wherein said step of introducing said abbreviated timing
3 delay and said extended timing delay includes executing said simulated
4 synchronous sequence under respective best case timing delay and worst
5 case timing delay scenarios in a system simulation environment, said system
6 simulation environment having timing characteristics indicative of said
7 particular system of interest.

1 9. (currently amended) ~~The storage medium~~ The computer-implemented
2 method of claim 7 further including adapting said simulated synchronous
3 extended-delay sequence as said simulation synchronous sequence when
4 there is not an acceptable number of said overlapping second time intervals.

1 10. (currently amended) ~~The storage medium~~ The computer-implemented
2 method of claim 7 wherein said step of providing said simulated asynchronous
3 sequence includes selecting said clock period to have a duration that
4 corresponds to a tester clock period of an IC tester.

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1 11. (currently amended) ~~The storage medium~~ The computer-implemented
2 method of claim 2 further including selectively fixing a sampling instance in
3 one of said overlapping sampling time intervals to correspond to a rising edge
4 of a tester clock period of an IC tester.

1 12. (currently amended) ~~A computer-readable medium having executable~~
2 ~~instructions for driving a test~~ A test vector generator for generating a
3 synchronous sequence of test vectors ~~such that said executable instruction~~
4 ~~and test vector generator are cooperative to comprise~~ comprising:
5 a computer-implemented simulation module that is enabled to
6 generate a simulation synchronous sequence of states under a system
7 simulation environment, said simulation synchronous sequence including a
8 plurality of timing regions for identifying operations of an integrated circuit (IC).
9 design;
10 a computer-implemented delay module that is enabled to
11 introduce short delays and long delays to said simulation synchronous
12 sequence to respectively generate asynchronous short-delay sequence and
13 asynchronous long-delay sequence, each of said short delays and said long
14 delays being timing delays associated with at least one of an integrated circuit
15 (IC) and an IC tester;
16 [[an]] a computer-implemented overlaying module that is
17 configured to provide a first state overlapping time interval and a second state
18 overlapping time interval by respectively comparing a plurality of base periods
19 of said asynchronous short-delay sequence and comparing a plurality of base
20 periods of said asynchronous long-delay sequence;
21 a computer-implemented duplication module that is configured
22 to incorporate said first state overlapping time interval into a first sequence of
23 said base periods and to incorporate said second state overlapping time
24 interval into a second sequence of said base periods to respectively generate
25 a synchronous short-delay sequence and a synchronous long-delay
26 sequence; and
27 a computer-implemented sequence overlaying module that is
28 configured to time align said synchronous short-delay sequence and said
29 synchronous long-delay sequence to detect a plurality of overlapping
30 sampling intervals for locating said synchronous sequence of test vectors.

1 13. (currently amended) ~~The computer-readable medium of claim 12 wherein~~
2 ~~said executable instructions are configured such that~~ The test vector
3 generator of claim 12 wherein said short delays are related to a best case
4 chip-load timing delay of said IC and a best case tester-load timing delay of
5 said IC tester.

1 14. (currently amended) ~~The computer-readable medium of claim 13 wherein~~
2 ~~said executable instructions are configured such that~~ The test vector
3 generator of claim 13 wherein said long delays are related to a worst case
4 chip-load timing delay of said IC and a worst case tester-load timing delay of
5 said IC tester.

1 15. (currently amended) ~~The computer-readable medium of claim 12 wherein~~
2 ~~said executable instructions are further cooperative with said test vector~~
3 ~~generator to define a~~ The test vector generator of claim 12 further comprising
4 a computer-implemented verification module that is configured to execute said
5 synchronous sequence of test vectors under said short delays and said long
6 delays for verifying timing correctness.

1 16. (currently amended) ~~The computer-readable medium of claim 12 wherein~~
2 ~~said executable instructions are configured such that~~ The test vector
3 generator of claim 12 wherein said system simulation environment is
4 independent of any delay associated with said IC and said IC tester.

1 17. (currently amended) ~~The computer-readable medium of claim 12 wherein~~
2 ~~said executable instructions are configured such that~~ The test vector
3 generator of claim 12 wherein said base period is a time interval that is
4 equivalent to a tester period of said IC tester.

1 18. (currently amended) ~~A program storage device having computer-~~
2 ~~executable code for implementing a~~ A computer-implemented method for
3 converting asynchronous states into synchronous states to generate a
4 synchronous sequence of test vectors for verifying functionality of a simulated
5 integrated circuit (IC) design comprising:
6 providing a simulation synchronous sequence of states;
7 generating an asynchronous short-delay sequence of first
8 periods and an asynchronous long-delay sequence of second periods,
9 including inserting short delays and long delays into said simulation
10 synchronous sequence, said short delays and said long delays characterizing
11 timing delays of at least one of said simulated IC and a tester,
12 detecting a short-delay overlapping time interval and a long-
13 delay overlapping time interval, including correlating a plurality of said first
14 periods to identify said short-delay overlapping time interval and correlating a
15 plurality of said second periods to identify said long-delay overlapping time
16 interval;
17 generating a synchronous short-delay sequence of states by
18 forming a succession of substantially identical base periods that include a
19 state and said short-delay overlapping time interval;
20 generating a synchronous long-delay sequence of states by
21 forming a succession of substantially identical base periods that include a
22 state and said long-delay overlapping time interval; and
23 generating said synchronous sequence of test vectors, including
24 time-aligning said synchronous short-delay sequence and said synchronous
25 long-delay sequence and identifying overlapping timing envelopes of states
26 within corresponding said base periods of said synchronous short-delay and
27 long-delay sequences.

1 19. (currently amended) ~~The program storage device~~ The computer-
2 implemented method of claim 18 wherein said step of inserting said short
3 delays and said long delays includes respectively introducing best-case timing
4 delays of said simulated IC and worst-case timing delays of said simulated IC.

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- 1 20. (currently amended) ~~The program storage device~~ The computer-
- 2 implemented method of claim 19 wherein said step of inserting said short
- 3 delays and said long delays includes respectively introducing best-case timing
- 4 delays of said tester and worst-case timing delays of said tester.